NAME :KRISHMA

DEPARTMENT:COMPUTER ENGINEERING DESIGNATION: LECTURER

SEMESTER:4TH

SUB:COMPUTER ORGANIZATION

TEACHING LOAD:4(L)

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| **WEEK**  **NO.** | **THEORY DAY** | **TOPICS COVERED** |
| 1 | 1 | CPU organization, general register organisation,stack organization |
| 2 | Three address, two address |
| 3 | One address ,zero address |
| 4 | RISC Instruction |
| 2 | 1 | Addressing modes: Immediate,register,direct |
| 2 | Indirect,relative,indexed |
| 3 | CPU Design: Microprogrammed.vs hard wired control |
| 4 | Reduced instruction set computer |
| 3 | 1 | CISC characteristics |
| 2 | RISC characteristics |
| 3 | Comparison between above two |
| 4 | Revision & Assignment |
| 4 | 1 | Test |
| 2 | Memory Hierarchy |
| 3 | RAM and ROM chips |
| 4 | Memory address map |
| 5 | 1 | Memory connection to CPU |
| 2 | Auxillary Memory |
| 3 | Cache memory &Virtual memory |
| 4 | Seminar |
| 6 | 1 | Memory Management hardware |
| 2 | Read and write operation |
| 3 | Revision & Assignment |
| 4 | Test |
| 7 | 1 | Introduction to I/O organisation |
| 2 | Functions of BIOS |
| 3 | Testing and Initialization |
| 4 | Configuring the system |
| 8 | 1 | Introduction to modes of data transfer |
| 2 | Programmed I/O |
| 3 | Synchronous & Asynchronous |
| 4 | Seminar |
| 9 | 1 | Interrupt |
| 2 | DMA data transfer |
| 3 | Revision & Assignment |
| 4 | Test |
| 10 | 1 | Introduction to Architecture of Multi processor systems |
| 2 | Forms of parallel processing |
| 3 | Parallel processing and pipelines |
| 4 | Seminar |
| 11 | 1 | Characteristics of multiprocessor |
| 2 | Purpose of Multi processor systems |
| 3 | Seminar |
| 4 | Interconnection network |
| 12 | 1 | Time shared common bus |
| 2 | Multi ports memory |
| 3 | Cross bar switch |
| 4 | Multi stage Switching networks |
| 13 | 1 | Hyper cube structures. |
| 2 | Revision & Assignment |
| 3 | Seminar |
| 4 | Test |
| 14 | 1 | Revision |
| 2 | Revision |
| 3 | Test |
| 4 | Test |
| 15 | 1 | Revision |
| 2 | Test |
| 3 | Revision |
| 4 | Revision |